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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/650,340 | 08/28/2003 | Thomas L. Drabenstott | 800.0130 | 6843 |

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| EXAMINER | |
|---|---|
| PAN, DANIEL H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/650,340 | DRABENSTOTT ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *34-40,53 and 56-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-40,53 and 56-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 34-40,53,56-61, 62-66 are presented for examination. Claims 1-33, 41-52,54,55 have been canceled.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 34, 53 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 9 of U.S. Patent No. 6,366,999. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

Claims 34,53 are generic to the species of invention covered by claims 1 , 9 of the patent. Thus, the generic invention is "anticipated" by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) . This court's predecessor has held that, without a terminal disclaimer, the

species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller , 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 1, 53 are properly rejected under the doctrine of obviousness-type double patenting (see In re Goodman (CA FC) 29 USPQ2d 2010).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 34-40, 53, 56-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibrino et al. (6,061,707) in view of Pawate et al. (5,528,550).

3. AS to claim 34, 53, Dibrino disclosed a system for generating complex conditions formed by a Boolean combination (see the AND gate) of relations comprising:

a) an arithmetic unit [25 ADDER] which receives at least two operands from a register file [24] (see fig.2, see the operands 11 and 12, see the two inputs to ADDER);

b) instruction control lines derived from a registered instruction in a processor pipeline (see the pipeline in col.3, lines 17-29 for pipeline processors ), the instruction control

lines including conditional execution control lines to control conditional operation as specified in an instruction (see the operand portions 11 and 12 in fig.2);

c) the arithmetic unit producing a result [SUM] and a latched arithmetic scalar condition state [carry] ,

d) a first latch [27] for holding the arithmetic scalar condition state [carry] for the instruction after the instruction has finished its execution state',

e) a second latch [28] connected to the conditional execution control lines for holding instruction control signals (see the 0 and 1 shift count in fig.3) for the instruction after the instruction has finished its execution state',

f) an arithmetic condition flag generation unit [27] for providing a Boolean combination {end-around carry} of a present state (see carry input to AND 27) with a previous state (see the shift count output to AND 27).

4. Dibrino did not specifically show the ACF (arithmetic flags) latch for storing the previous state and feeding back the previous state back to ACF generation unit as claimed. However, Pawate disclosed a system for feeding a previous arithmetic state of an arithmetic operation (see the direct feedback path from the accumulator in fig.3, see also col.6, lines 16-34). It would have been obvious to one of ordinary skill in the art to use Pawate in Dibrino for including a latch for storing and feedback the previous state as claimed because the use of Pawate could provide Dibrino the ability to accept the arithmetic conditions at predetermined point of processing ,such as accumulating the previously or lastly set results, directly for the updated arithmetic operation, thereby , reducing the hardware overheads, and therefore increasing processing

efficiency of the arithmetic operation, and it could be done by configuring the arithmetic latch of Pawate into Dibrino with modified control parameters, such as the R/W port number of the latch, so that the specific arithmetic latch of Pawate for feeding back the previous result could be recognized by Dibrino, and in doing so, provided a motivation.

5. Dibrino is used as primary reference because it showed clearly the Boolean combination of arithmetic conditions. Pawate is used to supplement the teaching of the ACF latch (see the accumulator) for storing and feeding back the arithmetic states.

6. AS to claims 35, 40,56,61, Pawate's latch was also programmer visible because it was associated with search instruction (see col.5, lines 40-60).

AS to claims 36,39, 57, Pawate also included a branch logic (see the branch logic in Table I).

7. As to claim 37, 58, Pawate also included a scalar latch ( shifter with the bus interface) switchbly connected to a first scalar latch [ register 58] (see fig.3).

8. As to claims 38,59, Pawate also included a controllable multiplexer for switching arithmetic state (see fig.3 [MUX]).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 62 , 64, 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Dibrino et al. (6,061,707) .

10. Dibrino taught at least a processing system comprising:

a) an arithmetic unit [ADDER 25] receiving at least two operands from a register file [11][12] , performing an operation on the at least two operands, and producing a result [Sum] and an arithmetic scalar condition state [carry]

b) conditional execution control signals (see shift count 0 and 1 in fig.3) derived from an instruction in an instruction pipeline to control conditional operation as specified in the instruction (see the pipeline instruction processing in col.3, lines 17-29 for pipeline processors).; and an arithmetic condition flag generation unit [27] for receiving both the conditional execution control signals [shift count from 28] and the arithmetic scalar condition state [output carry from Sum] , and for providing a present selected state of a plurality of arithmetic condition flags (see the ANDed end carry result in fig.2).

11. As to claim 64, Dibrino also included at least a carry.

12. As to claim 65, Dibrino did to explicitly show the compare instruction as claimed. However, it showed a compare logic circuit (see AND 27). Since no specific format or the hardware structure of the compare instruction ahs been reflected into the claim, it is read as any means capable of doing comparison operation, and it is also believed that

in order to operate the AND circuit 27 in Dibrino , it must have some form of command to active the compare operation, and therefore, for the above reasons m, it is found anticipated by Dibrino.

13. Claim 63 ,66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibrino et al. (6,061,707) in view of Pawate et al. (5,528,550).

14. As to claim 63, limitations od parent claim 62 have been discussed in paragraph 10, therefore, it will not be repeated herein. Dibrino did not specifically show the storage unit for storing the previous state of ACFs and feeding back the previous state back to ACF generation unit as claimed. However, Pawate disclosed a system for storing and for feeding a previous arithmetic state of an arithmetic operation (see the direct feedback path from the accumulator in fig.3, see also col.6, lines 16-34). It would have been obvious to one of ordinary skill in the art to use Pawate in Dibrino for including a latch for storing and feedback the previous state as claimed because the use of Pawate could provide Dibrino the ability to accept the arithmetic conditions at predetermined point of processing ,such as accumulating the previously or lastly set results, directly for the updated arithmetic operation, thereby , reducing the hardware overheads, and therefore increasing processing efficiency of the arithmetic operation, and it could be done by configuring the arithmetic latch of Pawate into Dibrino with modified control parameters, such as the R/W port number of the latch, so that the specific arithmetic latch of Pawate for feeding back the previous result could be recognized by Dibrino, and for the above reasons, provided a motivation.

15. Dibrino is used as primary reference because it showed clearly the arithmetic condition flag generation unit [AND 27] for receiving both the execution control signals (shift count) an the arithmetic scalar condition state (carry output from Sum). Pawate is used to supplement the teaching of the ACF latch (see the accumulator) for storing and feeding back the arithmetic states.

16. As to claim 66, Pawate also included a branch control logic (see the branch logic in Table I).

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Fernando (5,802,360) is cited for the teaching of a set of ACF arithmetic flags [PSW flags] that store the results of one or more conditions (see the 8 bit PSWOP register storing at least the C, V bits in col.4, lines 35-43).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*21 Century Strategic Plan*

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PRIMARY EXAMINER
GROUP